INVERSE DUAL CONVERTER (IDC) FOR HIGH POWER DC-DC APPLICATIONS

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A new family of dc-dc converters, suitable for high power dc-dc conversion is presented. The inverse dual converter (IDC) is capable of continuous voltage step-up or step-down control over a wide range and without the need of a transformer.

1. INTRODUCTION

DC-DC power conversion at low to medium power levels is a mature technology. Several classical and new topologies exist which use MOSFETs or BJTs for active current switching. The primary advantage of these topologies is that at very high frequencies, they can reduce reactive element sizes. However, these converters do not scale up efficiently when the power requirements extend to hundreds of kW or MW range. Resonant converters are among the few available dc-dc converters suitable for high power applications due to their natural commutation and soft switching ability. Examples of such converters include the series resonant converter (SRC) [1], all quasi-resonant converters [2] as well as the pseudo-resonant full-bridge converter [3]. However, resonant converters require careful matching of the operating frequency to the resonant tank components and any magnetic saturation or other unexpected drift in resonant frequency can result in operation failure. In these converters input and output capacitive filters are required to handle large ripple currents and the voltage and current stresses on the devices are also significant. Moreover, voltage step-up or step-down is not possible without a transformer.

Furthermore, smaller size and lower weight is a highly desirable feature in the area of power conversion, especially in aerospace applications. These constraints can only be met by reducing the transformer size and LC filter components. Primarily, this requires operation at higher switching frequencies and reduction in device switching losses by applying some form of soft-switching technique. The inverse dual converter (IDC) is a new topological concept in dc-dc power conversion which is specifically suitable for high power. This family of converters uses the technique of complementary commutation that eliminates the need of external commutation circuitry. In this method the firing of one thyristor commutates the complementary one. However, its frequency can be changed over a wide range because it does not depend on resonance for its operation. Furthermore, continuous voltage step-up or step-down control is possible over a very wide range without any transformers.

This paper describes the basic operation of the simplest IDC circuit. Analytical treatment of the converter, leading to the understanding of its dynamics and design equations are also given. This analysis is based on gyrator theory [4] whose use in power electronics is illustrated in the paper. Experimental verification of the analysis is done on the simple single phase IDC. Finally, the paper gives some of the more sophisticated members of the IDC family and mentions their characteristics and possible applications.

2. THE IDC CIRCUIT

The inverse dual converter (IDC) is basically a modification of the inductor converter bridge (ICB) circuit, shown in Fig. 1 [5,6]. The ICB is a two quadrant power supply developed for superconductive energy storage magnets [7]. The current source dc-dc converter circuit of ICB has been modified to a voltage source dc-dc converter in the IDC, shown in Fig. 2. Due to the small component values of L_S, L_L and C_L compared to the ICB the circuit response

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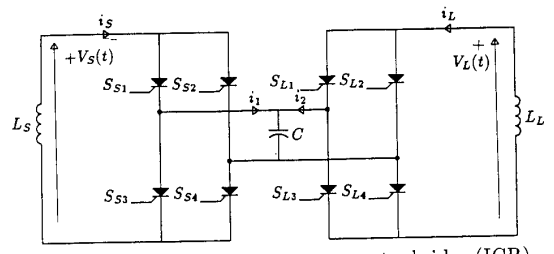

Fig. 1 The single phase inductor converter bridge (ICB) circuit

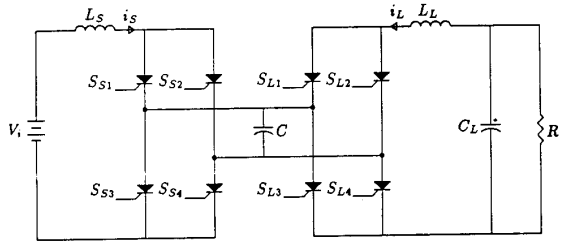

Fig. 2 The single phase inverse dual converter (IDC)

time is much shorter and the desired output voltage can be maintained by active control.

In the converter of Fig. 2, a clockdriven sequence of pulses with constant switching intervals drives the converters of the IDC. The switching sequence on the source converter is $S_{S1}S_{S4}, S_{S2}S_{S3}, S_{S1}S_{S4}$ etc. and the same switching sequence and frequency is used on the load side. The source and load side converter switching events need not be synchronized but must be of the same frequency. Proper design and control guarantees continuous conduction in the input and output inductors and also proper commutation of the switching elements by the ac capacitor, C. The capacitor on the ac link serves two purposes. It temporarily stores the energy to be transferred from one side to the other and also supplies the reverse voltage required for commutation of switches between S_1S_4 and S_2S_3 on each converter. Output voltage control and input current continuity is accomplished by two control variables: the common converter frequency and the difference of phase between the two converters. As the name implies, the IDC is exactly the inside out dual (inverse) of the conventional dual converter, in which the ac voltages are on the outside and the dc is the link.

The operation of the IDC is closely related to the ICB and a basic review of the latter is a helpful introduction to IDC. The ICB is a current source dc-dc converter system for reversible energy transfer between two high Q inductors. Quadro-metric [5] and state space averaging techniques have been applied [8] to obtain an average solution of the ICB circuit.

The coil voltages $V_S(t)$ and $V_L(t)$ averaged over a cycle have been determined to be,

$$V_S = -L_S\dot{I}_S = kI_L \tag{1}$$

$$V_L = -L_L\dot{I}_L = -kI_S \tag{2}$$

with

$$k = \frac{\phi - (\phi^2/\pi)}{\omega C}, \qquad 0 < \phi < \pi \tag{3}$$

where I_S and I_L are the average coil currents over the same cycle, ω is the angular frequency of the converter and ϕ is the load converter advance angle.

The average load power in a lossless one-phase ICB was shown to be,

$$< P >= kI_SI_L$$

or,

$$< P >= \frac{I_SI_L}{\omega C}(\phi - \frac{\phi^2}{\pi}), \qquad 0 < \phi < \pi \tag{4}$$

The process of energy transfer in the ICB can also be effectively implemented from a voltage source converter instead of a superconducting coil. In the IDC the superconducting coils have been replaced by two filter inductors and the voltage source at the input is the source of energy. The energy can be transferred to the load using the same principle as in ICB. Depending on which of the switches are conducting there are four distinct topologies identified as $14^S14^L, 14^S23^L, 23^S23^L$ and 23^S14^L (the superscripts represent the source side and load side). The operating waveforms of the single phase IDC with a phase difference between the source and load side converters are shown in Fig. 3.

The inverse dual converter is inherently a capacitor commutated converter with the capacitor acting as the voltage transfer element. The complementary commutation, provided by the ac capacitor, C, allows the use of SCRs. Therefore, the power rating of IDC can be scaled up, by design, to very high (MW) levels, using the well known HVDC converter technology. Furthermore, gate turn-off switches, such as GTOs or MCTs, can be used instead of SCRs. The combined current commutation and gate turn-off will allow efficient converter switching at much higher frequencies than those possible with SCRs. Thus, the filter sizes can be further reduced in certain high power applications.

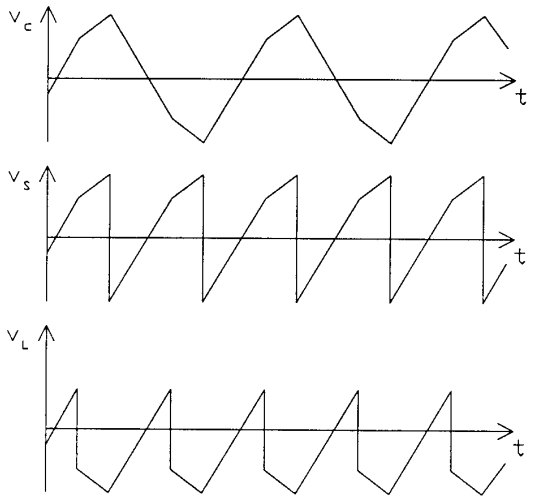

Fig. 3 The voltage waveforms: (i) Link capacitor voltage, v_c, (ii) Voltage across the source converter, v_S, (iii) Voltage across the load converter, v_L

3. MODELING OF IDC

The key to the detailed analysis of the inverse dual converter is the gyrator theory. A gyrator, similar to an ideal transformer, is a realizable network that couples an input port to an output port through a gyrostatic coefficient. It is a lossless and storageless two-port network which transforms one-port networks into their dual with respect to their gyration conductance. For example, an input voltage source is viewed as a current source at the gyrator output and vice versa. Similarly, a capacitance is seen as an inductance and so on. The circuit symbol for the basic gyrator appears in Fig. 4 and the defining equation is,

$$\begin{aligned} i_1 &= g v_2 \\ i_2 &= -g v_1 \end{aligned} \tag{5}$$

where g is called the gyration conductance and has the unit $\frac{1}{\Omega}$.

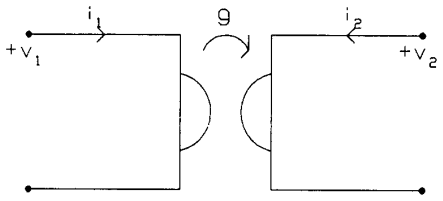

Fig. 4 Symbolic representation of a gyrator

The gyrator realization of networks started long ago but the application was limited only to small signal circuits. The efficiency requirements for signal processing circuits are not as rigorous as power processing circuits and gyrator realization of circuits operated at signal levels was not too difficult. During the last decade the switchmode power conversion techniques operated at high frequency such as buck, boost, buck-boost and flyback converters are in effect gyrator realizations of power processing circuits.

The gyrator realization of power electronic converters is based on the assumption that the output power equals instantaneous input power, $P_o = P_i$, and is called the POPI circuit [4]. This, in fact, is a loss-free realization of the ideal gyrator along with a signal $h(t)$ driving the POPI circuit which is the control element. In the following it will be shown that converters with a link capacitor as in the ICB or IDC behave naturally as a gyrator without any extra control components as required in the above realizations.

In the case of ICB, from equations (1) and (2) we can write,

$$\frac{< v_L >}{< i_S >} = -\frac{< v_S >}{< i_L >} = k$$

where k is defined in equation (3). Comparing with the gyrator equation,

$$\frac{< v_2 >}{< i_1 >} = -\frac{< v_1 >}{< i_2 >} = \frac{1}{g}$$

The gyration conductance is,

$$g = \frac{1}{k} = \frac{\omega C}{\phi - (\phi^2/\pi)} \tag{6}$$

Observing that the switching topology of the IDC is the same as that of the ICB, the gyration conductance of both ICB and IDC will be the same.

The averaged gyrator model of the IDC is very helpful in analyzing the circuit. The circuit can be modeled viewing from both the source side and the load side. Fig. 5 shows the equivalent circuit with the source V_i and the

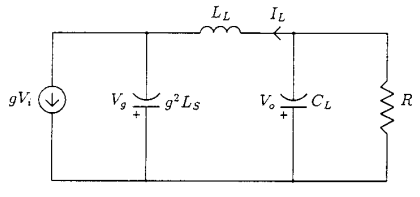

Fig. 5 Gyrator equivalent circuit of the IDC viewed from the load side

inductor L_S transformed to the load side.

In steady state,

$$I_L = gV_i \tag{7}$$

$$V_o = I_L R = gV_i R \tag{8}$$

The dc gain is given by,

$$\frac{V_o}{V_i} = gR = \frac{\omega C}{\phi - (\phi^2/\pi)} R \tag{9}$$

Power flow is,

$$< P >= \frac{I_S I_L}{g} = \frac{I_S I_L}{\omega C}(\phi - \frac{\phi^2}{\pi}) \tag{10}$$

The input quantities can be obtained by drawing the equivalent circuit viewed from the source side as shown in Fig. 6. The steady state input current is given by,

$$I_S = \frac{V_i}{1/g^2 R} = V_i g^2 R \tag{11}$$

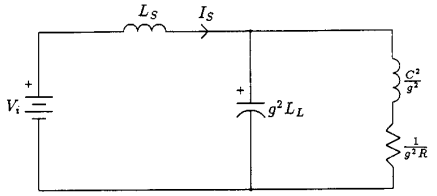

Fig. 6 Gyrator equivalent circuit of the IDC viewed from the source side

4. DESIGN OF IDC

The gyrator model can be effectively used to set the design rules of an IDC circuit. The complete design of IDC includes finding the ac link capacitance,C, source inductance,L_S, load inductance,L_L, and the filter capacitance,C_L as well as specifying the voltage and current ratings of these components.

The gyration conductance,g can be found for a converter with given power ratings and specified output voltage using Eqn. (10) and choosing an appropriate operating phase the value of the link capacitance can be obtained from Eqn. (6).

To find the source inductor let us consider the instantaneous voltage that appear across it as shown in Fig. 7.

The current ripple Δi_s across the inductor is given as,

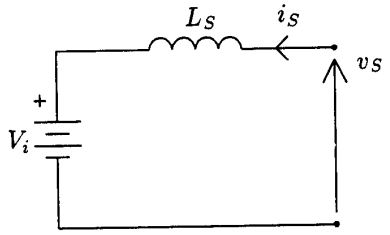

Fig. 7 The voltage appearing across the inductor,L_S

$$\Delta i_s = \frac{1}{L_S}\int_0^{t_c}(V_i - v_s)dt \tag{12}$$

where $t_c = t$ where $V_i = v_s(t)$. In most cases, dc-dc converters are applied either to step-up or step-down a voltage. The difference in magnitudes of the source and load inductor currents will then be significant and for illustration purposes we can concentrate on one. Let us consider a step-up converter in which case, $I_S >> I_L$ and the ripple current turns out to be,

$$\Delta i_s = \frac{I_S}{32 C L_S f^2} \tag{13}$$

The source inductor is then given by,

$$L_S = \frac{1}{32 C r f^2} \tag{14}$$

where, $r = \Delta i_s / I_S$ = the ripple factor; f = operating frequency.

A similar derivation and an additional assumption that the ripple voltage equals the output dc voltage at $t = T/4$ will lead to an expression for the load inductor ,

$$L_L = \frac{n}{32 r f^2 C} \tag{15}$$

where, $n = I_S / I_L$ = the ratio of input and output average currents.

These assumptions lead to the fact that the inductor design does not depend on the operating phase. However, in practice, the current ripple does depend on the operating phase but this ripple is negligible .

Assuming that all of the ripple current passes through the capacitor and not through the load the output filter capacitor can be estimated by the following equation,

$$C_L = \frac{\Delta i_l}{8 f_r \Delta V_{CL}} \tag{16}$$

where, f_r = ripple frequency;ΔV_{CL} = ripple voltage in capacitor.

The details of these derivations are discussed in [9].

5. CONTROL OF IDC

An important feature of the gyrator modeling is that it describes completely both the steady state and transient behavior of the IDC. It must be mentioned here that steady state and transient behavior, referred to here, is the averaged behavior over one switching cycle.

The IDC is essentially a power supply and the output voltage and power must be controlled independently of the input voltage. The gain formula in Eqn. (9) shows that the control can be accomplished by two elements, namely operating phase and frequency. These two variables which are evidently coupled can be modulated in a coordinated fashion to achieve dynamic control. Of the infinite combinations of phase and frequency , for a given gain, the control operating point (ϕ, ω) is chosen such that the average source inductor current,I_S (given by Eqn. 11) is maintained constant at a specific level. The control operating point at any instant of time is determined by solving Eqns. (9) and (11). Therefore, the system controller is capable of controlling the voltage gain and input current (or output voltage) smoothly through a wide range. Notice that both voltage step-up and step-down is possible continuously without the need for a transformer. The control block diagram of an IDC system is shown in Fig. 8. The above basic control strategy can be applied to many specific dc-dc converter applications such as regulated output control, tracking output voltage control, constant input power control and many others.

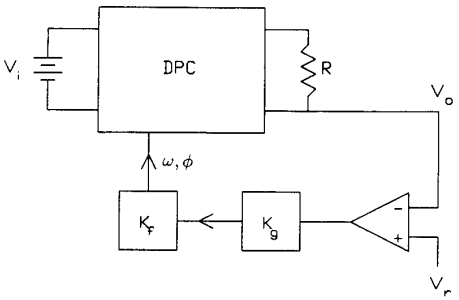

Fig. 8 Block diagram of an IDC control system

The alternative to the above phase and frequency control is the bang-bang control technique which can be used by setting $\phi = 90^0$ or $\phi = 90^0$ alternately. The bang-bang control was successfully implemented in ICB as described in [7]. Furthermore, a microprocessor control, with the combination of all the possible techniques, can be used to optimize the operation. In such case, a wide range of output voltage control will be possible.

6. THREE PHASE IDC

Several modifications of the basic single-phase IDC circuit can be conceived in order to minimize the size and weight of the IDC for aerospace applications. One way to produce a low input current ripple and output voltage ripple with the smallest filter components is the multiphase IDC as shown in Fig. 9.

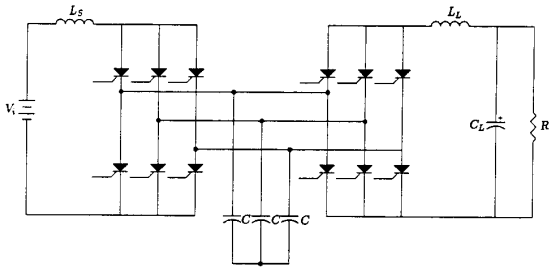

Fig. 9 Circuit diagram of a three-phase inverse dual converter (IDC)

The output filter component values of the three-phase IDC can be designed to be significantly less than that of the single-phase for the same system performance specifications. This, of course, is achieved, at the cost of additional switching elements and their support components. However, when weight and volume is the critical design constraint, careful tradeoff of silicon for inductance and capacitance must be studied.

The power relation and the gyration conductance for the three-phase IDC are given as follows:

$$
\begin{aligned}
< P > &= \frac{I_S I_L}{\omega C}(2\phi - \frac{3\phi^2}{2\pi}) \qquad for \quad 0 < \phi < \frac{\pi}{3} \\
< P > &= \frac{I_S I_L}{\omega C}(3\phi - \frac{3\phi^2}{\pi} - \frac{\pi}{6}) \qquad for \quad \frac{\pi}{3} < \phi < \frac{2\pi}{3} \\
< P > &= \frac{I_S I_L}{\omega C}(\phi - \frac{3\phi^2}{2\pi} + \frac{\pi}{2}) \qquad for \quad \frac{2\pi}{3} < \phi < \pi
\end{aligned}
\tag{17}
$$

The gyration conductance for the three-phase IDC is, therefore, given by,

$$g = \frac{\omega C}{2\phi - (3\phi^2/2\pi)} \quad for \quad 0 < \phi < \frac{\pi}{3}$$
$$g = \frac{\omega C}{3\phi - (3\phi^2/\pi) - (\pi/6)} \quad for \quad \frac{\pi}{3} < \phi < \frac{2\pi}{3} \quad (18)$$
$$g = \frac{\omega C}{\phi - (3\phi^2/2\pi) + (\pi/2)} \quad for \quad \frac{2\pi}{3} < \phi < \pi$$

For the $0 < \phi < \frac{\pi}{3}$ interval, comparing Eqn. (17) with Eqn. (10) we can assume, from a first order approximation, that the capacitor required for the three-phase IDC is twice the value of that required for the single-phase IDC of the same power. Furthermore, since there are three capacitors the peak voltage will be six times less. The ripple frequency for the three-phase IDC will be three-times greater and therefore from equations (14) and (15) the source and load inductors will be approximately 18 times smaller than that of the single phase IDC.

Another approach to reducing the filter requirements is the multipulsing technique. In these IDC systems, each side (source or load) consists of two or more basic converters in series. A similar arrangement exists on the load side of the IDC. The output filter requirements of multipulsed IDC can be reduced all the way to zero, for certain high power applications. This and other variations of IDC are the subject of a future paper on the subject.

7. EXPERIMENTAL RESULTS

A small $220W$ proof of principle single phase IDC set up was built in the Power Electronics Laboratory at Texas A&M University. Two $4mH$ inductors (L_S and L_L) were wound on the iron powder cores. The link capacitor values were between 0.5 and $3\mu f$ for different experiments. The frequency range for the experiments were between 2 and $5kHz$.

For $V_{in} = 109V$, $I_{in} = 1.75A$, $V_o = 100V$, $I_o = 1.68A$, $f = 2.4kHz$, $\phi = 90^0$ and $C = 1.39\mu f$, the estimated efficiency was 94%. Snubbers of $3\mu H$ were added to each thyristor currents. However, no dv/dt snubber was necessary.

The simulation results for $V_o = 60V$ and $\phi = 40^0$ for the single phase IDC are shown in figures 10a and 10b while the oscillograph obtained with the experimental unit for the input and output currents under the same operating condition appears in Fig. 11. The difference between the theoretical and experimental results comes from the circuit parasitics and lossy behavior of the experimental prototype.

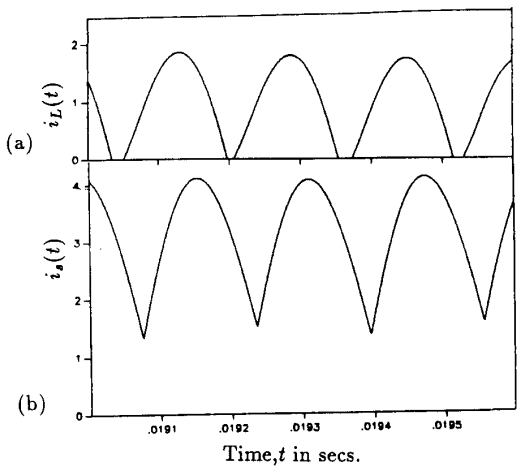

Fig. 10 Simulation results for the IDC for $V_o = 60V$, $C = 1.66\mu f$, $L_S = L_L = 4mH$, $C_F = 120\mu f$, $\phi = 40^0$ and $f = 3.1kHz$; a) load inductor current,i_L, b)source inductor current,i_S

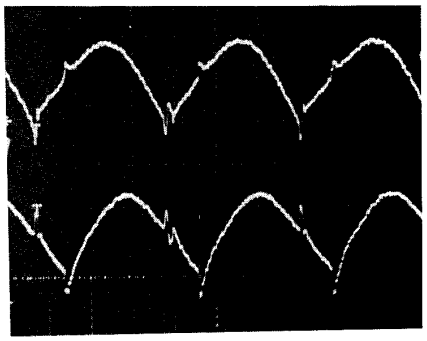

Fig. 11 Experimental results for the prototype IDC for $V_o = 60V$, $C = 1.66\mu f$, $L_S = L_L = 4mH$, $C_F = 120\mu f$, $\phi = 40^0$ and $f = 3.1kHz$;
upper trace: load inductor current,i_L (1A/div.)
lower trace: source inductor current,i_S (2A/div.)

For example, the parasitic capacitances across the coils cause a ringing whenever switching takes place. The ringing frequency was observed to be 3.5 MHz. The simulation and experimental input and output currents for the same operating condition as before but with a phase difference of 144^0 appear in Fig. 12 and Fig. 13 respectively.

The experimental IDC was designed with unity nominal gain and the phase angle was chosen as the control element to vary the output voltage. Although the gain is theoretically independent of the input and output voltages, in practice, different gain vs. phase characteristics were obtained at different voltage levels. The primary reason for

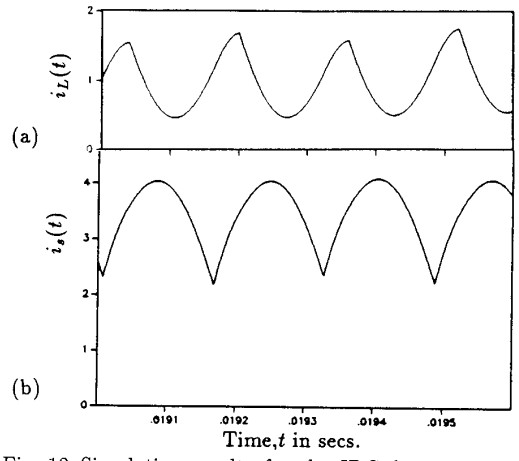

Fig. 12 Simulation results for the IDC for $V_o = 60V$, $C = 1.66\mu f$, $L_S = L_L = 4mH$, $C_F = 120\mu f$, $\phi = 144^0$ and $f = 3.1kHz$; a) load inductor current,i_L, b)source inductor current,i_S

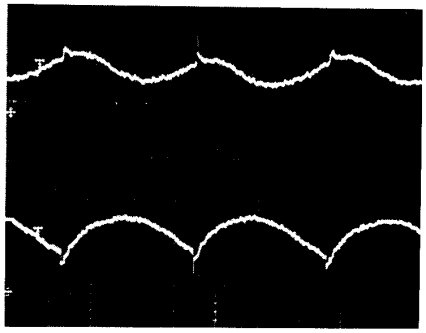

Fig. 13 Experimental results for the prototype IDC for $V_o = 60V$, $C = 1.66\mu f$, $L_S = L_L = 4mH$, $C_F = 120\mu f$, $\phi = 144^0$ and $f = 3.1kHz$; upper trace: load inductor current,i_L (1A/div.) lower trace: source inductor current,i_S (2A/div.)

this discrepancy is that practical gain is also a function of efficiency. It is also observed that, as the input power is increased the efficiency improves, the reason being that the conduction losses of thyristor are dominant at low power levels.

Further work is currently being carried out to develop a zero current switching inverse dual converter. It is expected that the zero switching operation of IDC will show similar behavior outlined in this paper.

8. CONCLUSION

The inverse dual converter (IDC), suitable for high power dc-dc conversion applications has been presented in this paper. The IDC is a voltage source converter with an ac link and has been derived from the circuit of inductor converter bridge (ICB) [10]. This capacitor commutated converter is capable of continuous voltage step-up or step-down control over a wide range without the need of a transformer. In addition to high frequency switching the converter is characterized by soft switching techniques reducing constraints on the ratings of the switches. The dual of this converter has also been studied in [11] but that converter needs forced turn-off switches for its operation.

The average model developed with the help of gyrator theory provides sufficient information for control strategies and design considerations. The results of gyrator modeling and computer simulation has been compared with experimental results obtained from a prototype IDC set up on laboratory testing conditions.

This paper also introduced the characteristics of some of the more sophisticated members of the IDC family.

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