Capacitively coupled converter (C3) for high power DC-DC conversion

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CAPACITIVELY COUPLED CONVERTER (C^3) FOR HIGH POWER DC-DC CONVERSION

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Abstract

The Capacitive Coupled Converter (C^3) is described for high power voltage source dc-dc applications. Its steady-state and dynamic behavior are analysed theoretically and by computer simulation. Factors affecting its operation and control are discussed and some design rules are presented. A proof of principle model of C^3 was constructed and its waveforms were recorded.

1. Introduction

A schematic diagram of the Capacitive Coupled Converter (C^3) is shown in Fig. 1. The basic concept of this converter was proposed by Simon And Bronner of Princeton Plasma Physics Laboratory,in 1967 [1]. This converter concept was specifically intended for high power energy transfer between two current sources (two large inductors). However, they suggested ignitrons for switching elements. The first experimental capacitive fly-back converter circuit , using SCRs for power switches, was proposed by Dick and Dustman [2].

In Fig. 1. we present a modification of Simon and Bronner's converter concept which is appropriate for voltage source dc-dc high power processing. A low power variation of this circuit which uses a high frequency transistor for S_1 and a diode for S_2 has also been presented under the the name Cúk converter [3].However, the hard current turn-off nature of switch S_1 in that converter makes it inappropriate for high power applications. Our proposed Capacitor Coupled Converter uses capacitive commutation of both S_1 and S_2 switches. Therefore, SCRs can be used to implement these switches and the power capability of the converter can be expanded by orders of magnitude. If a high frequency design is required to reduce reactive element sizes, then high power gate turn-off devices, such as the GTO, ZTO or MCT can be used. Since these devices will have to switch at zero current (subsequent to capacitive commutation), their switching losses and switching speeds can be significantly improved beyond the common applications of these devices. Furthermore, the symmetrical topology of our proposed converter, makes it bilateral (two-quadrant) power converter and regenerated load energy can be transferred to the source. Note that C^3 is both a voltage step-up and step-down converter and can be controlled in both zones.

2. Principle of Operation

The operation of C^3 circuit during a typical cycle is as follows. When S_1 is conducting and S_2 is not, the capacitor, C_1, is being charged from or discharged into the load side inductor, L_2, depending on the polarity of its initial charge. At the same time, current in L_1 is being conducted through S_1. When S_2 is conducting and S_1 is not, the capacitor is being charged from or discharged into the source side inductor, L_1, depending on the initial charge on the capacitor. At the same time the load side inductor current is being conducted through S_2. The voltage waveforms for a typical cycle with $I_1 > I_2$ are shown in Fig. 2. By proper design of the inductors and frequency , continuous current is maintained in both L_1 and L_2, over a switching period. The coupling capacitor, C_1, voltage waveform is a combination of charging by currents I_1 and I_2. The negative slope corresponds to the interval when S_1 is conducting and the load side current, I_2, discharges the capacitor from $+V_o$ to $-V_m$. The positive slop corresponds to the interval when S_2 is conducting and the source side current, I_1, charges the capacitor from $-V_m$ to $+V_o$. Note that the coupling capacitor voltage is made to alternate in polarity so that both S_1 and S_2 can be commutated. However, for efficient energy transfer, this capacitor is highly biased to one side. To summarize, in a typical converter cycle a small amount of source energy is transferred to the source inductor, L_1, (S_1 is on) and the same amount of energy is transferred from capacitor, C_1, to the load side. In the next subcycle (S_2 is on), the small amount of source inductor excess energy is transferred to the capacitor C_1, while some of the load inductor excess energy is transferred to the load capacitor, C_2, and R. Therefore, the capacitor, C_1 serves two functions. One as intermediate energy buffer and the other as a commutation capacitor. For a low input-output current ripple operation the capacitor, C_1, energy is much smaller than the inductive energy in L_1 and L_2 and this is ensured by design. Power and voltage control is achieved by varying the converter operating period and the peak voltages of C_1 within one period. Several operating and control methods are possible as discussed in references [4] and [5].

Other variations of the basic Capacitive Fly-back Converter have been studied in [6,7] for high power and [8] for low power.

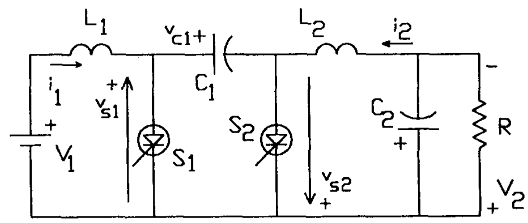

Figure 1 : Schematic of capacitor coupled converter.

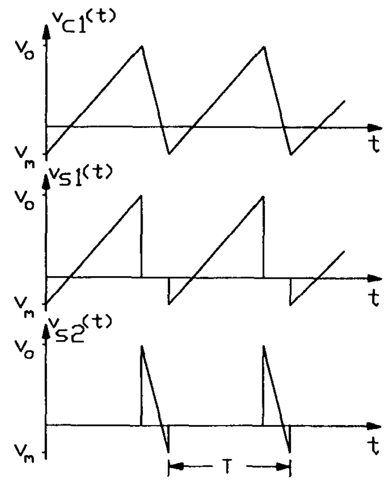

Figure 2 : Voltage waveforms for capacitive coupled converter (C^3) when $I_1 > I_2$.

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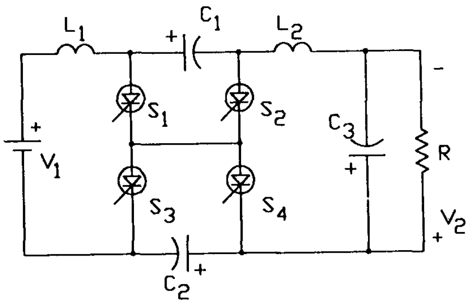


Figure 3: Schematic of the Dual Capacitive Coupled Converter Circuit.

For example, Figure 3. shows the schematic of a dual capacitive coupled converter which helps reduce the input-output current ripple and provides more degrees of freedom in control.

3. Analysis of Steady-State Operation

To obtain a stable operation in steady-state the following three conditions must be satisfied.

1 - The average of the voltage across S_1, $< v_{s1} >$, must be equal to the input voltage.

$$< v_{s1} > = V_1 \tag{1}$$

2 - The average of the voltage across the S_2, $< v_{s2} >$, must be equal to the output voltage.

$$< v_{s2} > = V_2 \tag{2}$$

3 - The rate of energy transferred by the capacitor C_1 must be equal to the rate of the energy consumed by the load R.

$$\frac{1}{2}C_1V_o^2 - \frac{1}{2}C_1V_m^2 = \frac{V_2^2}{R}T \tag{3}$$

where V_o is the positive peak value of the capacitor C_1 voltage and V_m is the negative peak, as shown in v_{c1} of Fig. 2, and T is the switching period.

These three conditions can also be formulated as follows.

$$V_1 = \frac{V_o - V_m}{2}(\frac{1}{1+G}) \tag{4}$$

$$V_2 = \frac{V_o - V_m}{2}(\frac{G}{1+G}) \tag{5}$$

$$\frac{2RC_1}{T} = \frac{G^2}{(1+G)^2}\frac{V_o - V_m}{V_o + V_m} \tag{6}$$

where G is the voltage gain (V_2/V_1).

4. Design of C^3

To guarantee commutation in the loop consisting of $S_1 - C_1 - S_2$, in Figure 1., V_m must be set by design. Similarly, to guaratee over voltage protection of the switches, V_o is also set by design. For the rated or nominal operating conditions V_1, V_2 and R are given. For a given voltage gain, $G = V_2/V_1$, in equation (6), we can set the value of the coupling capacitor, C_1, to get the period, T, which is within the switching speed rating and acceptable input/output filter design sizing to meet the ripple specs. For steady state nominal operation the coupling capacitor voltage threshold comparator is set at V_m and V_o and this will also guarantee all of the above considerations.

Control of C^3

Two variables may cause small signal perturbation around the steady state operating point:

1- Load changes from R_1 to R_2 (Regulation): By keeping V_o and V_m constant the gain, G, is kept constant from expression (4). This means that V_2 is also constant ($G = V_2/V_1$) and the small change of load R is corrected by a small changes of period T, according to equation (6). As long as change of R is small, change of T will be small and this should not have a large impact on the input-output filter effectiveness and the resulting ripples.

2- Change of gain, G (Control): Suppose V_1 is constant and V_2 must change to V_2' which is close to V_2. The following equation can be obtained from equations (4) and (5)

$$V_o = 2(V_2 + V_1) + V_m \tag{8}$$

In this equation, it is seen that V_m can be kept constant to guaratee commutation and V_o is changed to accomodate the new gain. This will cause small modulation of period T as in the previous case.

The dynamics of the above small signal control can be analysed from average models which are similar to those already developed for this converter topology [3]. However, here the switching period is not constant but changes in the small.

Large control transients can be handled by large signal control. An example is start-up transient where the gain goes from zero to a finite number such as 3. From equation (8) it is observed that if V_1 and V_m are constant a large change in V_2; e.g., from zero to V_2,will require a large change in V_o (from zero to V_o). However, the input resonant loop consisting of $V_1 - L_1 - C_1 - S_1$ puts a theoretical limit on the largest V_o achievable in any one switching cycle. For example, for the first start-up switching cycle, this limit is approximately

$$V_{o1} \geq V_1. \tag{9}$$

where V_{o1} is the maximum obtainable voltage in the first resonant cycle, which is ideally equal to $2V_1$. If this V_{o1} is much smaller than the steady state V_o than several cycles of start-up transients are required, each one taking advantage of the largest growth in V_o that can be achieved in one cycle, so that the steady state is reached in the shortest transient time. However, this then requires a set of transient V_o commands to be fed to the threshold comparator of the coupling capacitor voltage. The steps of V_o to be fed to the comparator depend on the C^3 circuit dynamics and can only be derived by simulation or cycle to cycle circuit analysis. This dynamic behavior cannot be predicted from the previously mentioned small signal average model and must be obtained from actual C^3 circuit including its parasitic resistances, etc. The reason is that the switching period is allowed to change widely over a short time.

Design Example

In the following a non optimized design example will be presented for illustration. The C^3 to be designed has the following specifications.

Input voltage, $V_1 = 270V$
Output voltage, $V_2 = 28V$
Output Power $P = 25KW$
Switching Frequency, $f_s = 50KHz$
Gain, $G = 0.104$.

The load resistance will be $R = V_2^2/P = 28^2/25 \times 10^3 = 0.0314 ohms$

Assuming $V_m/V_o = 0.1$, from equation (6) the coupling capacitor, C_1, is

$$C_1 = \frac{T}{2R}\frac{G^2}{(1+G)^2}\frac{V_o - V_m}{V_o + V_m}$$

$$= \frac{20 \times 10^{-6}}{2 \times 0.0314}\frac{0.104^2}{(1+0.104)^2}\frac{1-0.1}{1+0.1} = 2.31 \times 10^{-6}\ F$$

$$= 2.31\ \mu F$$

From equation (4) and $V_o/V_m = 0.1$, V_o and V_m are 662 V and 66.2 V, respectively.

L_1 and L_2 can be found for a given set of ΔI_1 and ΔI_2 current ripples by the following approximate formulas.

$$L_1 = \frac{(V_o - V_1)^2 T}{2\Delta I_1(V_o + V_m)}(\frac{1}{1+G}) \tag{9}$$

$$L_2 = \frac{(V_o - V_2)^2 T}{2\Delta I_2 (V_o + V_m)} \left(\frac{G}{1+G}\right) \qquad (10)$$

For 20% and 40% input and output current ripple, respectively, $L_1 = 0.1\ mH$ and $L_2 = 1.6\ \mu H$.

Similarly, the output filter capacitor can be found from

$$C_2 = \frac{\Delta I_2 . T}{8 \Delta V_2}, \qquad (11)$$

where ΔV_2 is the given peak-to-peak output voltage ripple. For 4% output voltage ripple, C_2 is 800 μF.

5. Simulation Results

A computer model was developed for simulation which was based on the switched converter topology. Runga-Kutta method was used to perform the solution of the circuit equations.

Figures 4,5 and 6 show the simulation results for the C^3 which was designed in the previous section.

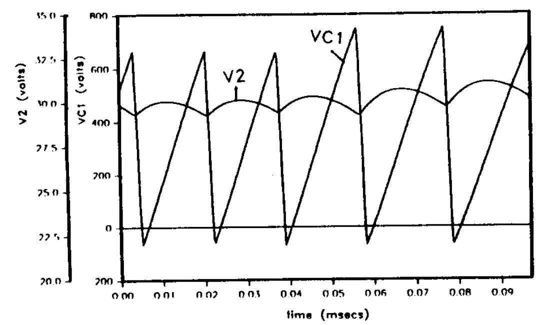


Figure 4: Small signal transient of coupling capacitor voltage, v_{c1}, and output voltage, v_{c1}, due to gain change.

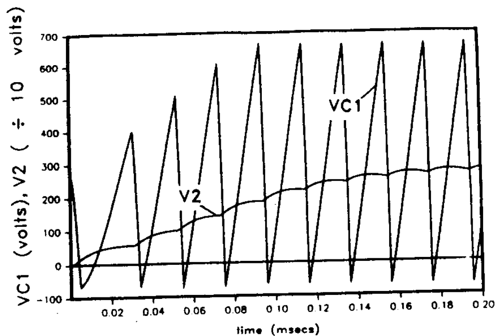


Figure 5 : Large signal start-up transient of coupling capacitor voltage, v_{c1} and output voltage, v_2.

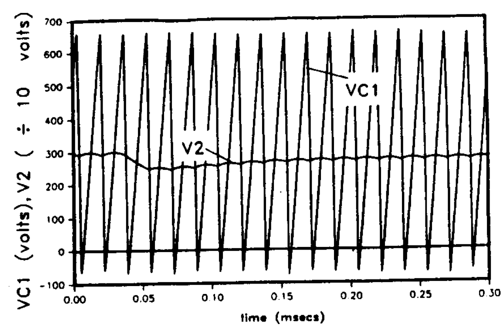


Figure 6 : Small signal transient of coupling capacitor voltage, v_{c1}, and output voltage due to load change.

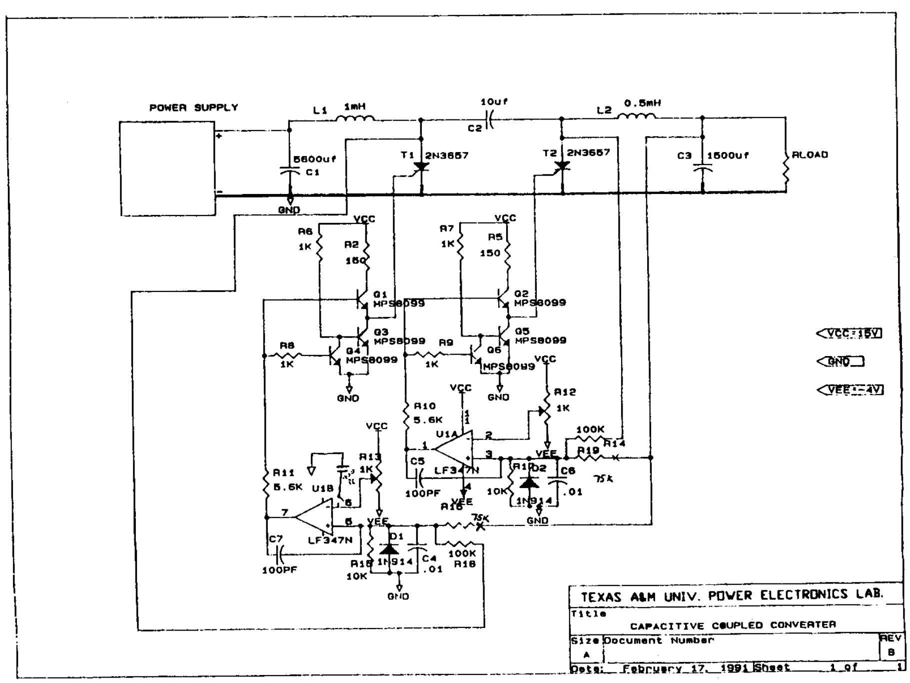
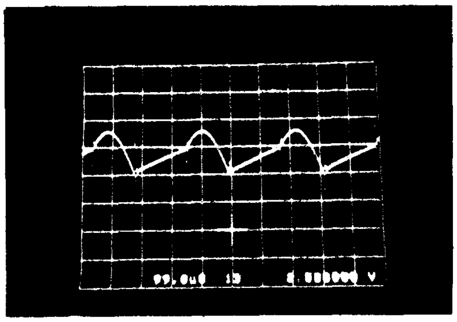
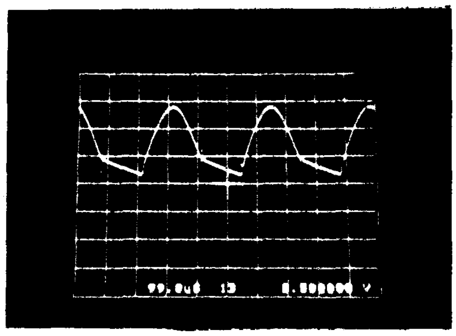


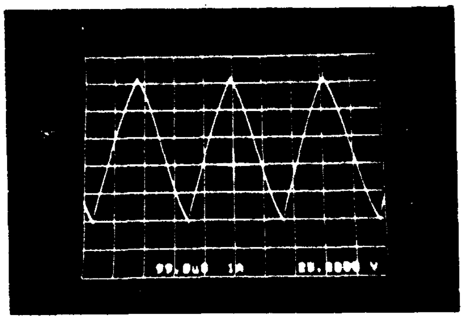
Figure 7: The experimental capacitor coupled converter.



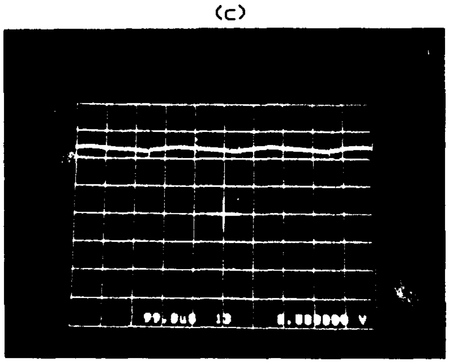
(a)



(b)



(c)



(d)

Figure 8 : Experimental waveforms of the C^3. a) Input current 2.5 A/div. b)Output inductor current, 2.5 A/div., c) The coupling capacitor voltage, 50 V/div., d) Output voltage 2.5 V/div. Time scale: 100 μs. Oscillograms are taken for $I_1 = 6$ A, $I_2 = 4.8$ A and G=1.13.

6. Experimental Results

A small exprimental C^3 was built for proof of principle in the Power Electronics Laboratory at Texas A&M University. This circuit and its component values are shown in Figure 7. The experimental waveforms are seen in Figure 8.

7. Conclusions

The C^3 circuit for high power DC-DC voltage source application is presented in this paper. This converter has been derived from the Single Flying Capacitor Converter, SFC, which was used in superconductive energy storage magnets [1,2]. The capacitor coupled converter is capable of controlled step-up and step-down control without the need of transformer. The combination of C^3's inherent current commutation and gate turn-off devices can lead to efficient, high frequency, high power (determined by the available switching devices) converters , with compact filters. The use of SCR's as the switching elements can lead to C^3 designs with virtually unlimited power capabilities.

Acknowledgement

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